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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,664	04/07/2004	Timothy Phua	1016-039	8017

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EXAMINER	
BREWSTER, WILLIAM M	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,664	PHUA ET AL.	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *15-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Claims 15-22 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 12 May 2005.

Applicant's election of claims 1-14 in the reply filed on 12 May 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-3, 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Long et al., US Patent No. 6,306,710 B1.

Long anticipates a manufacturing method for a semiconductor device comprising:

in fig. 3, forming layers of gate dielectric material 216 gate material 206, and, in fig. 15, cap material 296 on a semiconductor substrate;

in fig. 15, processing the cap material and a portion of the gate material to form a cap and a gate body portion;

in fig. 6, forming a wing, width of 222 to the bottom of 230, on the gate body portion from a remaining portion of the gate material, col. 5, lines 42-53;

in fig. 8, removing the gate dielectric material under a portion of the wing on the gate body portion to form a gate dielectric 202, col. 6, lines 22-34; and

in fig. 9, forming a lightly-doped source/drain region 242, 244 in the semiconductor substrate using the gate body portion and the wing, col. 6, line 22 - col. 7, line 24;

limitations from claim 2, the method as claimed in claim 1, in fig. 11, wherein forming the wing 230 includes rounding the outside edge thereof;

limitations from claim 3, the method as claimed in claim 1 further comprising:

in figs. 11 - 12, forming a first spacer 262 around the gate body portion and over the remaining portion of the gate material and the gate dielectric material; and in fig. 13, forming the lightly-doped source/drain region 242-244, additionally using the first spacer, wherein the doped source/drain regions 272-274 define the boundaries and the functionalities of the LDDs;

limitations from claim 7, the method as claimed in claim 1 further comprising, in fig. 14, forming a metal contact 286 over the gate body portion, 230, col. 9, lines 9- 20.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long as applied to claims 1-3, 7 above, and further in view of Chakravarthi et al., US Patent No. 6,797,593 B2.

Long does not teach using multiple spacers, but Chakravarthi does. Chakravarthi teaches:

limitations from claim 4, the method as claimed in claim 1 further comprising:

in fig. 5D, forming a first spacer, vertical sections of 426, around the gate body portion 406 and over the remaining portion of the gate material 404 and gate dielectric material 406;

forming a second spacer 410 around the first spacer;

in fig. 5B, removing the remaining portion of the gate material 404 except under, in fig. 5E, the first spacer, the second spacer, and the cap; and

removing the gate dielectric material 406 under the portion of the gate removes the gate dielectric material under the second spacer, col. 12, lines 47 - col. 13, line 35;

limitations from claim 5, the method as claimed in claim 4 further comprising:

in fig. 5I, forming a third spacer 444 around the gate body portion and the gate dielectric; and in fig. 5G, removing the first spacer and the second spacer;

limitations from claim 6, the method as claimed in claim 4 further comprising:

in fig. 5G, removing the first spacer and the second spacer;

in fig. 5I, forming a further spacer 444 around the gate body portion and the gate dielectric; and forming a source/drain region in the semiconductor substrate using the further spacer, including silicide contacts, col. 13, lines 17-35.

Chakravarthi gives motivation in col. 2, line 64 - col. 3, line 15. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Chakravarthi's process with Long's invention would have been beneficial because it forms an improved drain extension.

Claims 8, 9, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long in view of Wolf, V. I, pp. 191-4.

Long teaches a manufacturing method for a semiconductor device comprising:

in fig. 3, forming layers of silicon dioxide 216 or nitrided oxide material, amorphous or polycrystalline silicon 206, col. 4, lines 43-57, and, in fig. 15, a cap material 296, on a silicon substrate 204;

in figs. 14, 15, processing the cap material and a portion of the amorphous or polycrystalline silicon to form a cap and an amorphous or polycrystalline silicon gate body portion;

in fig. 6, forming an amorphous or polycrystalline silicon wing, between width of 222 tapering to base of 230, on the amorphous or polycrystalline silicon gate body portion 230 from a remaining portion of the amorphous or polycrystalline silicon to form an amorphous or polycrystalline silicon wing gate, col. 6, lines 22-34;

in fig. 8, removing the silicon dioxide or nitrided oxide material under a portion of the amorphous or polycrystalline silicon gate wing to form a gate dielectric 202, col. 6, lines 22 - 34;

in fig. 9, forming a lightly-doped source/drain region 242 - 244 in the semiconductor substrate using the amorphous or polycrystalline silicon wing gate, col. 6, line 22 - col. 7, line 24; and

in fig. 15, forming a poly metal dielectric layer, from lower portion of 296 and upper portion of 286 over the amorphous or polycrystalline silicon wing gate, col. 9, lines 9 - line 40;

limitations from claim 9, the method as claimed in claim 8, in fig. 11 wherein forming the amorphous or polycrystalline silicon gate wing includes rounding the outside edge thereof using a high temperature/high pressure oxidation 260, col. 7, lines 36 - 47, wherein 'high temperature/high pressure' is subjective to the observer;

limitations from claim 14, the method as claimed in claim 8 further comprising forming a metal contact, 286, over the amorphous or polycrystalline silicon gate body 230 portion, col. 9, lines 9- 20.

Long does not teach using nitride cap layers or spacers, but Wolf teaches using nitride. Wolf teaches using nitride and gives motivation on p. 191, fourth paragraph. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Wolf's process with Long's invention would have been beneficial because it is nearly impervious barrier to diffusion.

Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long in view of Wolf as applied to claims 8, 9, 14 above, and further in view of Chakravarthi.

Neither Long nor Wolf teach using multiple spacers, but Chakravarthi does. Chakravarthi teaches

limitations from claim 10, the method ms claimed in claim 8 further comprising:

in fig. 5D, forming a first spacer, vertical portions of 426, around the amorphous or polycrystalline silicon gate 404 body portion and over the remaining portion of the amorphous or polycrystalline silicon and the silicon dioxide 406 or nitrided oxide material; and

in fig. 5F, forming the lightly-doped source/drain region additionally using the first spacer, col. 12, line 47 - col. 13, line 35;

limitations from claim 11, the method as claimed in claim 8 further comprising:

forming a first spacer 426 around the amorphous or polycrystalline silicon gate body portion and over the amorphous or polycrystalline silicon and silicon dioxide or nitrided oxide material;

forming an oxide second spacer 410 around the first spacer;

in fig. 5B, removing the remaining portion of the amorphous or polycrystalline silicon 404 except under the nitride first spacer, the oxide second spacer, and the nitride cap; and, in fig. 5A, removing the silicon dioxide or nitrided oxide material removes the silicon dioxide or nitrided oxide material under the oxide second spacer to form a gate dielectric, 406;

limitations from claim 12, the method as claimed in claim 11 further comprising:

in fig. 5G, removing the first spacer and the oxide second spacer; and

in fig. 5I, further processing of the amorphous or polycrystalline silicon gate including an

amorphous or polycrystalline re-oxidation process, forming 444;

limitations from claim 13, the method as claimed in claim 11 further comprising:

in fig. 5G, removing the first spacer and the oxide second spacer;

in fig. 5I, forming an oxide further spacer around the amorphous or polycrystalline silicon gate and the gate dielectric; and

in fig. 5I, forming a source/drain region in the semiconductor substrate using the oxide further spacer, including silicide contacts, col. 13, lines 17-35.

Chakravarthi gives motivation in col. 2, line 64 - col. 3, line 15. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Chakravarthi's process with Long's invention would have been beneficial because it forms an improved drain extension.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

William M. Brewster

29 June 2005
WB